

SEMICONDUCTOR CHIP PACKAGE COMPRISING ENHANCED PADS

This application claims priority from Korean Patent Application 2001-5385, filed
5 February 5, 2001, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

10 The present invention relates to semiconductor packaging techniques and, more particularly, to a semiconductor chip package and a method of manufacturing the same.

2. Description of the Related Art

15 The trend in the electronics industry is toward producing lighter, thinner, faster, and more reliable multi-functional, high quality devices. A ball grid array (BGA) package has been introduced as one way of meeting these demands.

There are several ways to mount a BGA package on a board. When connection
terminals such as solder balls are used, poor adhesion between the semiconductor chip
package and the board has been a problem. Improvement in the reliability of these solder
20 joints between the semiconductor chip package and the board is therefore desired.

Several methods have been proposed as ways to improve the reliability of solder
joints. In one method, dummy balls are formed along the exterior of the solder balls. In
another approach, the size of solder balls or the shape of photo solder resist (PSR) is
controlled. And in another method, the material of solder balls is changed. Yet another
25 method is used in a conventional BGA package, as described below.

FIG. 1 is a cross-sectional view of a conventional BGA package 100. FIG. 2 is a plan
view of the bottom surface of a substrate 20 of the conventional BGA package 100 of FIG. 1.
FIG. 3 is an enlarged cross-sectional view of an area "A" of the BGA package 100 of FIG. 1.
Referring to FIGS. 1 through 3, in the conventional BGA package 100, a semiconductor chip
30 10 is mounted on the top surface of the substrate 20. Bonding pads 12 of the semiconductor
chip 10 are connected to metal wirings (not shown) of the substrate 20 via connectors 30 such
as bonding wires. The semiconductor chip 10 and the electrical connection parts including
the connectors 30 are encapsulated with a molding resin such as an epoxy molding compound
(EMC), thereby forming a package body 40. Ball pads 24 are formed on the bottom surface

of the substrate 20 and correspond to the metal wirings (not shown) of the substrate 20. The ball pads 24 are exposed from a photo solder resist (PSR) layer 22. A connection terminal 60 such as a solder ball is formed on each ball pad 24. The above-described package 100 is mounted on a board 50. The board 50 comprises ball lands 54 corresponding to the ball pads 24 and the connection terminals 60.

As shown in FIG. 3, the ball pads 24 of the package 100 are electrically connected to the ball lands 54 of the board 50 via the connection terminals 60. The connections of the connection terminals 60 to the ball pads 24 or to the ball lands 54 significantly affect the reliability of the package mounting. Since the above-described conventional BGA package 100 is mounted on the board by adhering the solder balls therebetween, the reliability of the package mounting is directly affected by the reliability of the solder joint of the connection terminals to the ball pads or to the ball lands.

As the size of the solder ball has become drastically reduced, the mounting height of the package on the board has also been reduced. This can result in cracks in the joints between the package and the board. In particular, among a group of solder balls arranged in a lattice shape, cracks occur more easily on the outermost solder balls. Furthermore, cracks occur most frequently along the long sides. Most of these cracks are caused by differences in the coefficients of thermal expansion.

Specifically, there is often a difference in the coefficients of thermal expansion between the solder balls and the ball pads or between the solder balls and the ball lands. Therefore, when the semiconductor chip package is tested under a temperature cycling (T/C) test, cracks occur in the joints between the solder balls and the ball pads or in the joints between the solder balls and the ball lands. Because cracks occur mainly in the joints between the solder balls and the substrate of the package, the industry would be greatly benefited by a method and structure that provides an improved joint force between the outermost solder balls and the ball pads of the substrate.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a semiconductor chip package configured to prevent cracks from forming between external connection terminals such as solder balls and ball pads.

Also, the present invention improves the solder joint reliability of a semiconductor chip package on a board by reducing the likelihood that its outermost solder balls will be damaged.

Accordingly, a substrate for forming a ball grid array (BGA) package comprises:
a substrate having a top surface and a bottom surface having ball pads, and a plurality of
enhanced pads formed on the bottom surface of the substrate. Each of the enhanced pads
includes one or more dummy pads coupled to one or more dummy patterns.

5 According to another embodiment of the present invention, a semiconductor chip
package comprises a substrate having a top surface for mounting a semiconductor chip
thereon and a bottom surface having ball pads. A plurality of enhanced pads are formed on
the bottom surface of the substrate. Each of the enhanced pads includes one or more dummy
pads coupled to one or more dummy patterns. External connection terminals such as solder
balls are formed on the ball pads. A molding resin encapsulates the semiconductor chip.

10 The ball pads are preferably arranged in a lattice shape on the bottom surface of the
substrate. The enhanced pads are formed on outer edges of the ball pad lattice. The
enhanced pads preferably comprise first, second, and third enhanced pads. Each of the first
enhanced pads may comprise one ball pad, two dummy pads, and dummy patterns for
15 connecting the ball pad to the dummy pads. Each of the second enhanced pads may comprise
one ball pad, one dummy pad, and a dummy pattern for connecting the ball pad to the dummy
pad. Each of the third enhanced pads may comprise two dummy pads and a dummy pattern
for connecting the dummy pads to each other.

20 BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the present invention will
be more readily understood through the following detailed description of preferred
embodiments made with reference to the accompanying drawings, wherein like reference
numerals designate like structural elements, and, in which:

25 FIG. 1 is a cross-sectional view of a conventional BGA package mounted on a board;

FIG. 2 is a plan view of the bottom surface of the board of the conventional board-
mounted BGA package of FIG. 1;

FIG. 3 is an enlarged cross-sectional view of an area "A" of the conventional board-
mounted BGA package of FIG. 1;

30 FIG. 4 is a cross-sectional view of a BGA package mounted on a board in accordance
with an embodiment of the present invention;

FIG. 5 is a plan view of the bottom surface of the board-mounted BGA package of
FIG. 4;

FIG. 6 is an enlarged cross-sectional view of an area "B" of the board of the board-mounted BGA package of FIG. 4;

FIGS. 7a to 7c are plan views illustrating several examples of enhanced pads of the present invention; and

FIGS. 8s to 8d are flow charts illustrating a method of mounting a BGA package on a board using the enhanced pads of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below with reference to the accompanying drawings. In particular, a board-mounted BGA package 200 according to an embodiment of the invention will be described in detail below with reference to FIGS. 4 through 6. FIG. 4 is a cross-sectional view of the board-mounted BGA package 200, including a chip 110 mounted on a substrate 120. FIG. 5 is a plan view of the bottom surface of the substrate 120 shown in FIG. 4. FIG. 6 is an enlarged cross-sectional view of an area "B" of FIG. 4 showing an interconnection between a board 150 and the BGA package 200.

Referring to FIGS. 4 through 6, in the BGA package 200, the semiconductor chip 110 is mounted on the top surface of the substrate 120. Bonding pads 112 of the chip 110 are connected to metal wirings (not shown) of the substrate 120 via electrical connectors 130, such as bonding wires. The semiconductor chip 110 and the electrical connectors 130 are encapsulated with a molding resin such as an epoxy molding compound (EMC), thereby forming a package body 140. Ball pads 124 are formed on the bottom surface of the substrate 120 and correspond to the metal wirings of the substrate 120. The ball pads 124 are exposed from, for example, a photo solder resist (PSR) layer 122. An external connection terminal 160 such as a solder ball is formed on each ball pad 124.

Enhanced pads 170 (including first, second, and third enhanced pads 170a, 170b, 170c) are preferably formed at outer edges of the bottom surface of the substrate 120. Each of the enhanced pads 170 comprises one ball pad 124, at least one dummy pad 174, and dummy patterns 172. The dummy patterns connect the ball pad 124 to the dummy pad 174. The detailed structure of the enhanced pads 170 will now be further described.

The BGA package 200 is mounted on the board 150. The board 150 comprises ball lands 154 and enhanced lands 180, corresponding to the ball pads 124 and the enhanced pads 170. As shown in FIG. 6, the ball pads 124 and the enhanced pads 170b of the BGA package 200 are electrically connected to the ball lands 154 and the enhanced lands 180b of the board

150 through the connection terminals 160, 162. The connection terminals 162 between the enhanced pads 170b and the enhanced lands 180b improve the reliability of the package mounting of this BGA package 200 over that of the conventional BGA package 100 (see FIGS. 1 through 3).

5 Still referring to FIG. 6, the connection terminals 162 are uniformly attached along substantially the entire surface area of the enhanced pads 170 and the enhanced lands 180. Although conventional dummy balls have been formed on dummy pads, since the dummy ball has the same size as the solder ball, this merely increases the size of the joint area or the package substrate without substantially increasing solder joint reliability. In the present
10 embodiment, each of the connection terminals 162 has at least two pads, i.e., the bond pad 124 and the dummy pad as well as patterns for connecting the pads to each other. The connection terminal 162 is therefore larger than the conventional structure, thereby improving the joint force. The connection terminals 162 between the enhanced pads 170 and the enhanced lands 180 thereby improves the solder joint reliability of the surface mount package
15 over the prior art.

As shown in FIG. 5, the enhanced pads 170 and the connection terminals 162 corresponding to the enhanced pads 170 are formed along the outer edges of the substrate 120. Compared to solder balls nearer the center of the substrate, cracks occur more easily in the outermost solder balls. By arranging the enhanced pads along the outer edges, the solder
20 joint reliability of the package is thereby improved. In other words, the enhanced pads formed along the outer edges of the substrate help prevent the occurrence of cracks of those solder balls. The solder balls are preferably all approximately the same size.

FIGS. 7a through 7c are plan views showing the various configurations of the enhanced pads 170 of this embodiment. Each of these enhanced pads 170 comprises at least
25 one dummy pad and a dummy pattern. Referring to FIGS. 5 and 7a, a first enhanced pad 170a comprises one ball pad 124, two dummy pads 174 arranged adjacent to the ball pad 124, and dummy patterns 172. The dummy patterns 172 connect the dummy pads 174 to the ball pad 124 and are preferably arranged perpendicular to each other. The first enhanced pads 170a are arranged in the corners of the substrate 120.

30 Referring to FIGS. 5 and 7b, a second enhanced pad 170b comprises a ball pad 124, a dummy pad 174 arranged adjacent to the ball pad 124, and a dummy pattern 172 that connects the dummy pad 174 to the ball pad 124. The second enhanced pads 170b are arranged along the short sides of the substrate 120. More particularly, each of the ball pads

124 located near a short side of the substrate 120 is connected to a single dummy pad 174 by the dummy pattern 172 to form a second enhanced pad 170b.

Referring to FIGS. 5 and 7c, a third enhanced pad 170c comprises a dummy pattern 172 connecting two dummy pads 174 to each other. The third enhanced pads 170c are arranged along long sides of the substrate. In other words, dummy pad pairs formed on long sides of the substrate 120 are connected together by a dummy pattern 172 to form the third enhanced pads 170c.

As described above, most of the dummy patterns 172 of this embodiment are arranged parallel to the long sides of the substrate 120. Since cracks, due to differences in the coefficients of thermal expansion between the substrate and the solder balls, occur most frequently along the long sides of the substrate 120, this configuration effectively prevent those cracks from forming. It should also be noted that enhanced lands 180 and ball lands 154 are formed on the board 150 to correspond to each of the enhanced pads 170. Since the enhanced lands 180 have the same configuration as the enhanced pads 170, the detailed description thereof will be omitted.

FIGS. 8a to 8d are flow charts illustrating a method of mounting a BGA package on a board 150 using the enhanced pads 170 of the foregoing embodiment of the present invention. The following method will be described with respect to the second enhanced pads 170b (of FIG. 7b). It should be noted, however, that the same method is also applicable to the first enhanced pads 170a as well as the third enhanced pads 170c.

Referring to FIG. 8a, the board 150 is prepared. To prepare the board 150, the ball lands 154 and the enhanced lands 180b are exposed from a photo solder resist (PSR) layer 152. Referring to FIG. 8b, a mask 168 having openings corresponding to the ball lands 154 and the enhanced lands 180b is mounted on the board 150. A solder paste 168 is then provided on the ball lands 154 and the enhanced lands 180b with a squeegee 166. The mask 168 is then removed.

Next, referring to FIG. 8c, the solder balls 160 are formed on the ball pads 124 and the dummy pads 174 of the substrate 120. Referring to FIG. 8d, the substrate 120 is formed on the board 150 by the solder balls 160, 162 and the solder paste 164 by a solder reflow process. According to this method, the connection terminal 162 is formed over an entire area of the second enhanced pad 170b including the ball pad 124, the dummy pad 174, and the dummy pattern 172.

Since a single connection terminal is formed using the whole area of the enhanced pad (including the ball pad, the dummy pads, and the dummy patterns), this preferred method of

the present invention effectively improves the reliability of the solder joint. Moreover, in this embodiment, most of the dummy patterns are arranged parallel to the long side of the substrate, along which cracks mainly occur, thereby more effectively preventing cracks. Thus, the foregoing embodiments of the present invention improve the reliability of the package mounting.

Although the present invention has been described in terms of preferred embodiments thereof, variations and modifications to the inventive concepts herein will be apparent to those skilled in the art. All such modifications fall within the spirit and scope of the present invention as defined in the appended claims.

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